

REVISIONS					
LTR	DESCRIPTION			DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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	PAGE		1	2	3	4	5	6	7	8	9	10	11	12											
PMIC N/A		PREPARED BY							DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO																
Original date of drawing YY-MM-DD		CHECKED BY							TITLE																
03-06-09		Phu H. Nguyen							MICROCIRCUIT, LINEAR, FAST-TRANSIENT- RESPONSE 1-A LOW DROPOUT VOLTAGE REGULATORS, MONOLITHIC SILICON																
		APPROVED BY							Thomas M. Hess																
		SIZE	CODE IDENT. NO.						DWG NO.														V62/03632		
		A	16236																						
		REV							PAGE 1 OF 12																

AMSC N/A

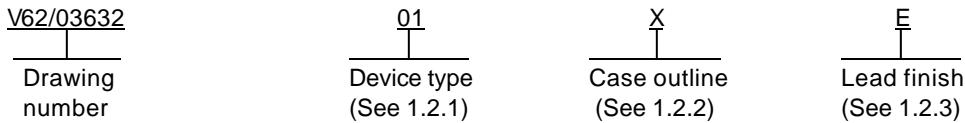
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5962-V033-03

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a fast-transient-response 1-A low dropout voltage regulators, with an operating temperature range of -40°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturers PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s). 1/

<u>Device type</u>	<u>Generic</u>	<u>Output voltage</u>	<u>Circuit function</u>
01	TPS76801-EP	+1.2 V to +5.5 V	Fast-transient-response 1-A low-dropout voltage regulator.
02	TPS76815-EP	+1.5 V	Fast-transient-response 1-A low-dropout voltage regulator.
03	TPS76818-EP	+1.8 V	Fast-transient-response 1-A low-dropout voltage regulator.
04	TPS76825-EP	+2.5 V	Fast-transient-response 1-A low-dropout voltage regulator.
05	TPS76827-EP	+2.7 V	Fast-transient-response 1-A low-dropout voltage regulator.
06	TPS76828-EP	+2.8 V	Fast-transient-response 1-A low-dropout voltage regulator.
07	TPS76830-EP	+3.0 V	Fast-transient-response 1-A low-dropout voltage regulator.
08	TPS76833-EP	+3.3 V	Fast-transient-response 1-A low-dropout voltage regulator.
09	TPS76850-EP	+5.0 V	Fast-transient-response 1-A low-dropout voltage regulator.

1.2.2 Case outline(s). The case outlines shall be as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	20	JEDEC MO-153	Plastic small outline

1.2.3 Lead finishes. The lead finishes shall be as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 2

1.3 Absolute maximum ratings. 2/

Input voltage range (V_I).....	-0.3 V to +13.5 V	<u>3/</u>
Voltage range at \overline{EN}	-0.3 V to $V_I + 0.3$ V	
Maximum PG voltage.....	+16.5 V	
Peak output current.....	Internally limited	
Continuous total power dissipation	See dissipation rating tables	
Output voltage (V_O) (OUT, FB)	+7.0 V	
Operating virtual junction temperature range (T_J).....	-40°C to +125°C	
Storage temperature range (T_{STG})	-65°C to +150°C	
ESD rating, (HBM)	2 kV	

Dissipation Rating Table – Ambient Temperatures

Case outline	Air Flow (CFM)	$T_A < 25^\circ C$ Power rating	Derating Factor	$T_A = 70^\circ C$ Power Rating	$T_A = 85^\circ C$ Power Rating
			Above $T_A = 25^\circ C$		
X 4/	0	2.9 W	23.5 mW/ $^\circ C$	1.9 W	1.5 W
	300	4.3 W	34.6 mW/ $^\circ C$	2.8 W	2.2 W
X 5/	0	3.0 W	23.8 mW/ $^\circ C$	1.9 W	1.5 W
	300	7.2 W	57.9 mW/ $^\circ C$	4.6 W	3.8 W

1.4 Recommended operating conditions.

Input voltage range (V_I).....	2.7 V to 10.0 V	<u>6/</u>
Output voltage (V_O).....	1.2 V to 5.5 V	
Output current (I_O).....	0 A to 1.0 A	<u>7/</u>
Operating virtual junction temperature range (T_J).....	-40°C to +125°C	<u>7/</u>

-
- 1/ Users are cautioned to review the manufacturers data manual for additional user information relating to these devices.
 - 2/ Stresses beyond those listed under "absolute maximum rating" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - 3/ All voltage values are with respect to network terminal ground.
 - 4/ This parameter is measured with the recommended copper heat sink pattern on a 1-layer PCB, 5 in x 5 in PCB, 1 oz. copper, 2 in x 2 in coverage.
 - 5/ This parameter is measured with the recommended copper heat sink pattern on a 8-layer PCB, 1.5 in x 2 in PCB, 1 oz. copper with layer 1, 2, 4, 5, 7, and 8 at 5% coverage (0.9 in²) and layers 3 and 6 at 100% coverage (6 in²). For more information, refer to the manufacturer technical brief SLMA002.
 - 6/ To calculate the minimum input voltage for your maximum output current, use the following equation:
$$V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$$
 - 7/ Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industry Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline(s). The case outline(s) shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.5.3 Block diagrams. The block diagrams shall be as specified on figure 3.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 4

TABLE I. Electrical performance characteristics.

Test	Test conditions $V_I = V_{O(\text{Typ})} + 1 \text{ V}$ $I_O = 1 \text{ mA}, \overline{\text{EN}} = 0 \text{ V}$ $C_O = 10 \mu\text{F}$ Operating at free air temperature range unless otherwise specified	Device type	Limits		Unit	
			Min	Max		
Output voltage (10 μA to 1 A load) <u>1/</u>	$T_J = 25^\circ\text{C}, \quad 1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$	01	V_O Typ		V	
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 1.5 \text{ V} \leq V_O \leq 5.5 \text{ V}$		0.98 V_O	1.02 V_O		
	$T_J = 25^\circ\text{C}, \quad 2.7 \text{ V} < V_{IN} < 10 \text{ V}$	02	1.5 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 2.7 \text{ V} < V_{IN} < 10 \text{ V}$		1.470	1.530		
	$T_J = 25^\circ\text{C}, \quad 2.8 \text{ V} < V_{IN} < 10 \text{ V}$	03	1.8 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 2.8 \text{ V} < V_{IN} < 10 \text{ V}$		1.764	1.836		
	$T_J = 25^\circ\text{C}, \quad 3.5 \text{ V} < V_{IN} < 10 \text{ V}$	04	2.5 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 3.5 \text{ V} < V_{IN} < 10 \text{ V}$		2.450	2.550		
	$T_J = 25^\circ\text{C}, \quad 3.7 \text{ V} < V_{IN} < 10 \text{ V}$	05	2.7 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 3.7 \text{ V} < V_{IN} < 10 \text{ V}$		2.646	2.754		
	$T_J = 25^\circ\text{C}, \quad 3.8 \text{ V} < V_{IN} < 10 \text{ V}$	06	2.8 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 3.8 \text{ V} < V_{IN} < 10 \text{ V}$		2.744	2.856		
	$T_J = 25^\circ\text{C}, \quad 4.0 \text{ V} < V_{IN} < 10 \text{ V}$	07	3.0 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 4.0 \text{ V} < V_{IN} < 10 \text{ V}$		2.940	3.060		
	$T_J = 25^\circ\text{C}, \quad 4.3 \text{ V} < V_{IN} < 10 \text{ V}$	08	3.3 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 4.3 \text{ V} < V_{IN} < 10 \text{ V}$		3.234	3.366		
	$T_J = 25^\circ\text{C}, \quad 6.0 \text{ V} < V_{IN} < 10 \text{ V}$	09	5.0 Typ			
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad 6.0 \text{ V} < V_{IN} < 10 \text{ V}$		4.900	5.100		
Quiescent current (GND current) <u>EN</u> = 0 V <u>1/</u>	$T_J = 25^\circ\text{C}, \quad 10 \mu\text{A} < I_O < 1 \text{ A}$	All	85 Typ		μA	
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad I_O = 1 \text{ A}$	All		125		
Output voltage line regulation ($\Delta V_O/V_O$) <u>1/</u> <u>2/</u>	$T_J = 25^\circ\text{C}, \quad V_O + 1 \text{ V} < V_I \leq 10 \text{ V}$	All	0.01 Typ		%/V	
		All	3 Typ		mV	
Load regulation			55 Typ		μVrms	
Output noise voltage	BW = 200 Hz to 100 kHz, $I_C = 1 \text{ A}$, $C_O = 10 \mu\text{F}, \quad T_J = 25^\circ\text{C}$	03	150 Typ		$^\circ\text{C}$	
Output current limit				2	A	
Thermal shutdown junction temperature		All	10 Typ			
Standby current	$T_J = 25^\circ\text{C}, \quad \overline{\text{EN}} = V_I, \quad 2.7 \text{ V} < V_I < 10 \text{ V}$	All	1 Typ		μA	
	$T_J = -40^\circ\text{C} \text{ to } 125^\circ\text{C}, \quad \overline{\text{EN}} = V_I, \quad 2.7 \text{ V} < V_I < 10 \text{ V}$			10		
FB input current	FB = 1.5 V	01	2 Typ		nA	

See notes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 5

TABLE I. Electrical performance characteristics - Continued.

Test	Test conditions $V_I = V_{O(Typ)} + 1\text{ V}$ $I_O = 1\text{ mA}$, $\bar{EN} = 0\text{ V}$ $C_O = 10\text{ }\mu\text{F}$ Operating at free air temperature range unless otherwise specified	Device type	Limits		Unit	
			Min	Max		
High level enable input voltage	$T_J = 25^\circ\text{C}$, $f = 1\text{ KHz}$, $C_O = 10\text{ }\mu\text{F}$	All	1.7		V	
Low level enable input voltage				0.9	V	
Power supply ripple rejection <u>1/</u>	$T_J = 25^\circ\text{C}$, $f = 1\text{ KHz}$, $C_O = 10\text{ }\mu\text{F}$		60 Typ		dB	
PG	Minimum input voltage for valid PG	$I_{O(PG)} = 300\text{ }\mu\text{A}$	1.1 Typ		V	
	Trip threshold voltage	V_O decreasing		92	$\%V_O$	
	Hysteresis voltage	Measured at V_O		0.5 Typ		
	Output low voltage	$V_I = 2.7\text{ V}$, $I_{O(PG)} = 1\text{ mA}$			V	
	Leakage current	$V_{(PG)} = 5\text{ V}$			μA	
Input current (\bar{EN})	$\bar{EN} = 0\text{V}$		-1	1	μA	
	$\bar{EN} = V_I$		-1	1	μA	
Dropout voltage <u>3/</u>	$T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$	06	500 Typ		mV	
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $I_O = 1\text{ A}$			825		
	$T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$	07	450 Typ			
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $I_O = 1\text{ A}$			675		
	$T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$	08	350 Typ			
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $I_O = 1\text{ A}$			575		
	$T_J = 25^\circ\text{C}$, $I_O = 1\text{ A}$	09	230 Typ			
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$, $I_O = 1\text{ A}$			380		

1/ Minimum IN operating voltage is 2.7 V or $V_{O(Typ)} + 1\text{V}$, whichever is greater. Maximum IN voltage 10 V.

2/ If $V_O \leq 1.8\text{ V}$ then $V_{I\max} = 10\text{ V}$, $V_{I\min} = 2.7\text{ V}$:

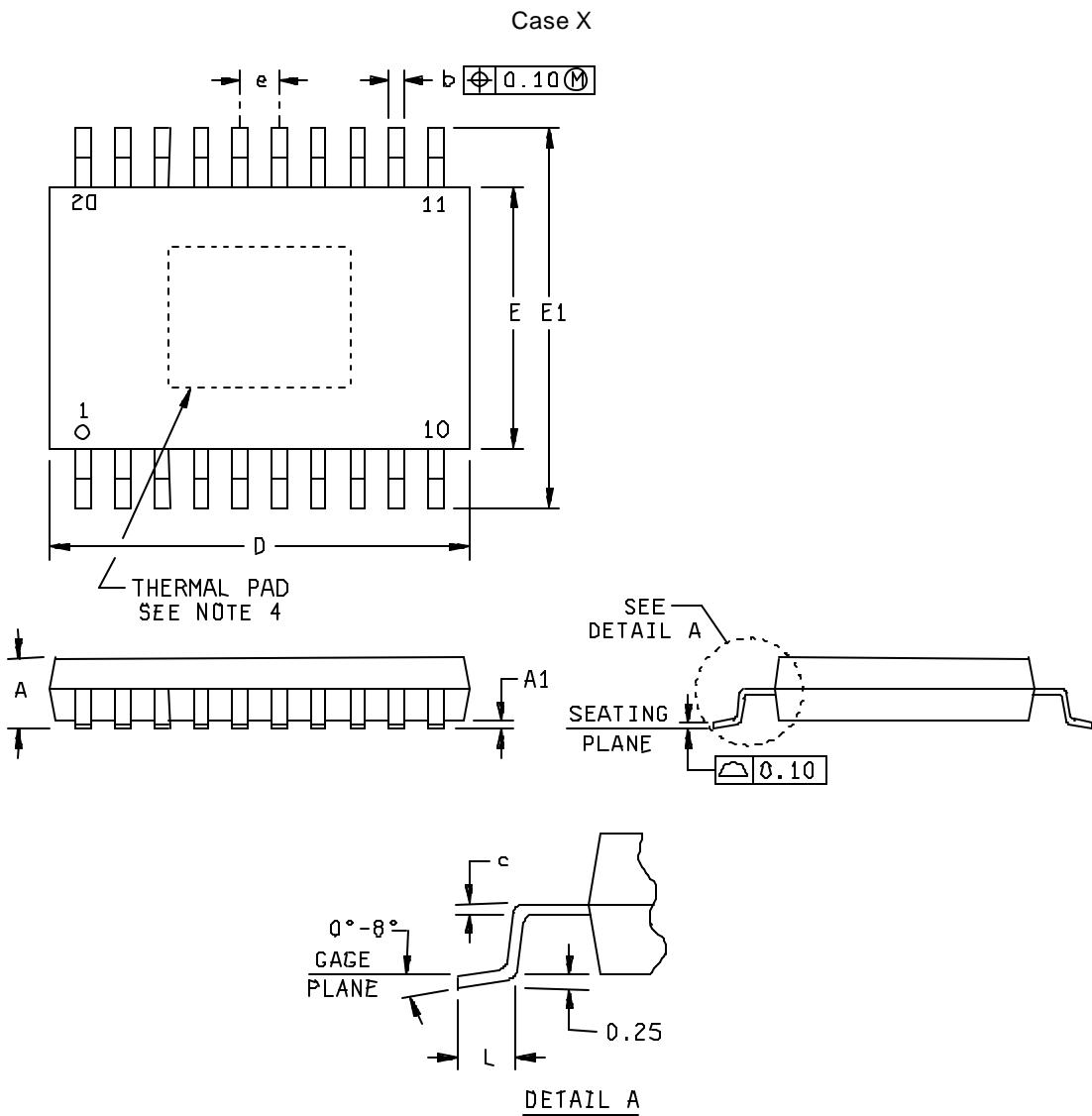
$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\max} - 2.7\text{V})}{100} \times 1000$$

If $V_O \geq 2.5\text{ V}$ then $V_{I\max} = 10\text{ V}$, $V_{I\min} = V_O + 1\text{ V}$:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\max} - (V_O + 1\text{V}))}{100} \times 1000$$

3/ IN voltage equals $V_{O(Typ)} - 100\text{ mV}$; Device type 01 output voltage set to 3.3 V nominal with external resistor divider. Device type 02, 03, 04 and 05 dropout voltage limited by input voltage range limitations (i.e., device type 07 input voltage needs to drop to 2.9 V for purpose of this test).

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 6



Notes:

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusions.
4. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
5. Falls within JEDEC MO-153.

FIGURE 1. Case outline.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 7

Case X

	Millimeters	
Symbol	Min	Max
A		1.20
A1	0.05	0.15
b	0.19	0.30
c	0.15 NOM	
D	6.40	6.60
E	4.30	4.50
E1	6.20	6.60
e	0.65 TYP	
L	0.50	0.75

FIGURE 1. Case outline - Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 8

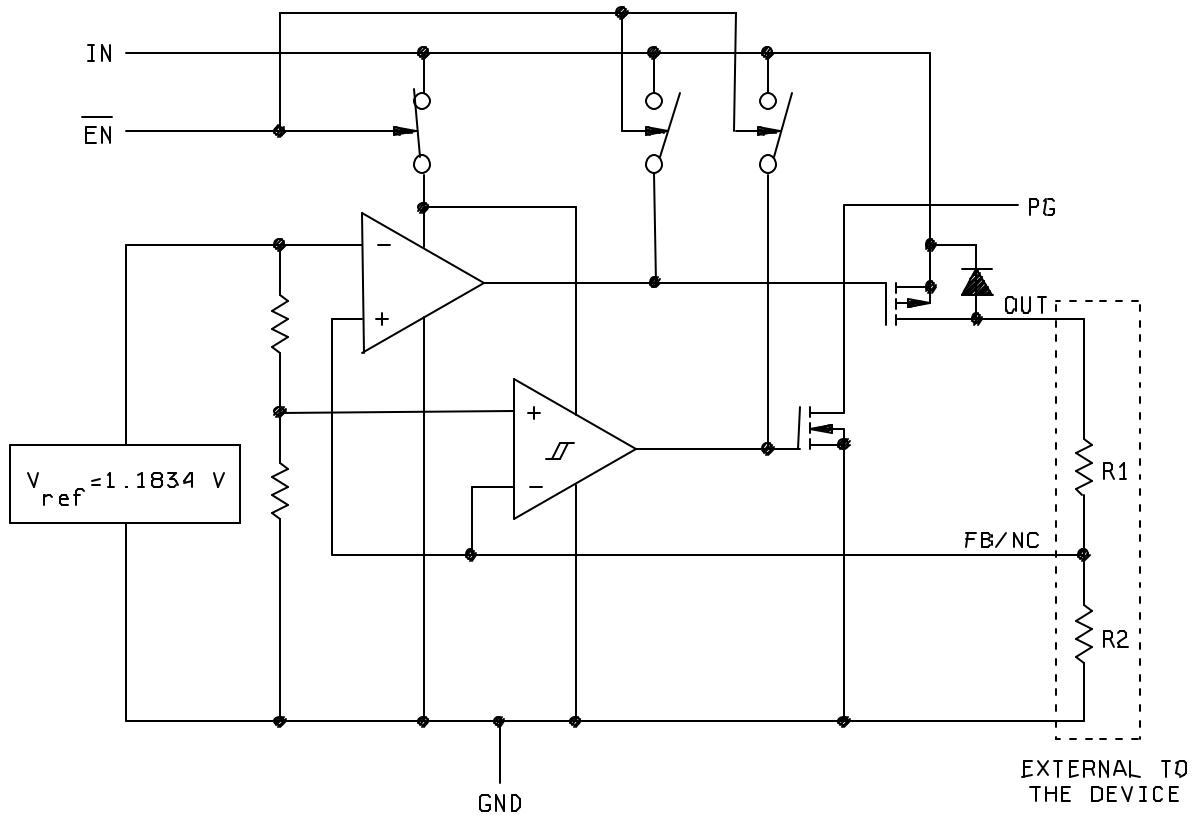
Case X

Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND/HSINK	11	GND/HSINK
2	GND/HSINK	12	GND/HSINK
3	GND	13	OUT
4	NC	14	OUT
5	EN	15	FB/NC
6	IN	16	PG
7	IN	17	NC
8	NC	18	NC
9	GND/HSINK	19	GND/HSINK
10	GND/HSINK	20	GND/HSINK

NC: No internal connection

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 9



Functional block diagram – adjustable version.

FIGURE 3. Block diagrams

**DEFENSE SUPPLY CENTER, COLUMBUS
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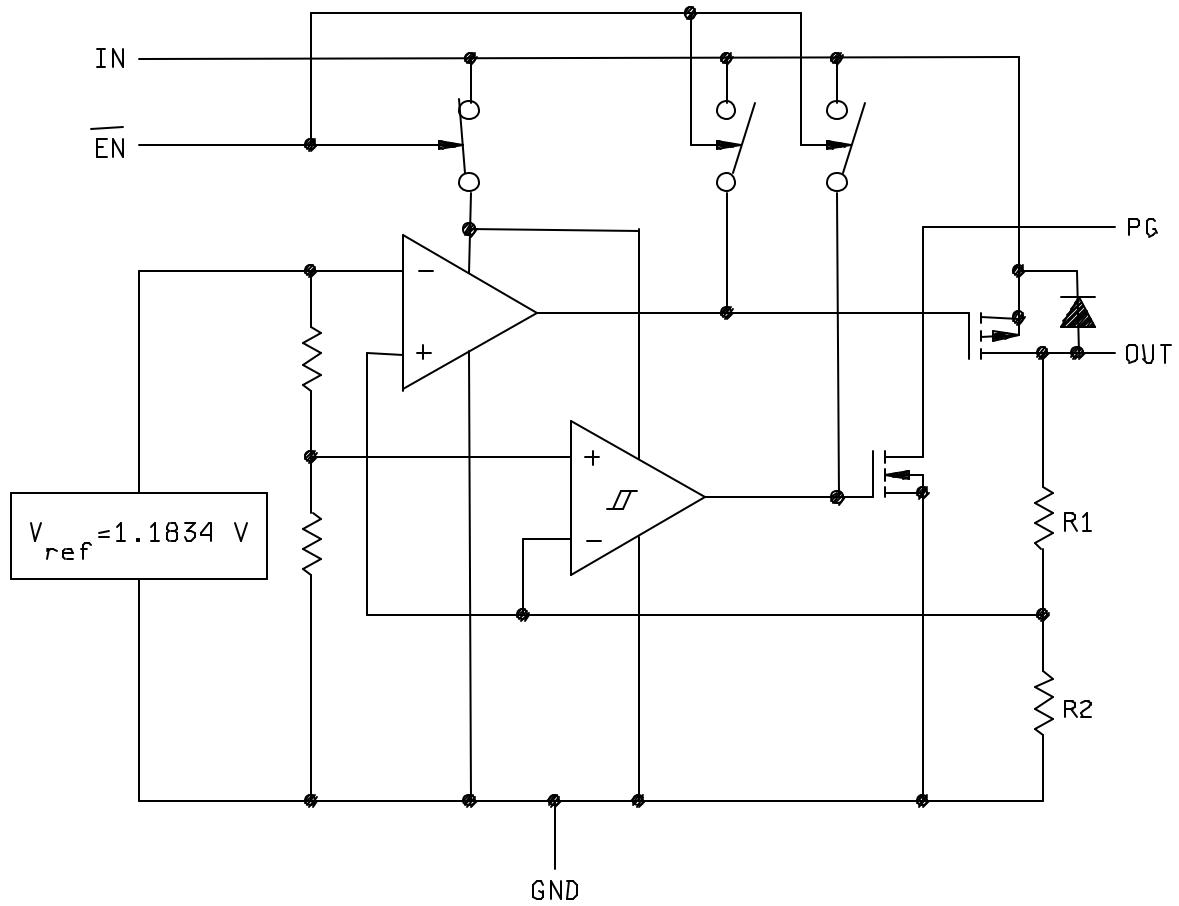
**SIZE
A**

**CODE IDENT NO.
16236**

**DWG NO.
V62/03632**

REV

PAGE 10



Functional block diagram – fixed voltage version.

FIGURE 3. Block diagrams – Continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 11

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5.0 PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6.0 NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number <u>2/</u>	Top-side marking
V62/03632-01XE	01295	TPS76801QPWPREP <u>3/</u>	76801EP
V62/03632-02XE	01295	TPS76815QPWPREP	76815EP
V62/03632-03XE	01295	TPS76818QPWPREP	76818EP
V62/03632-04XE	01295	TPS76825QPWPREP	76825EP
V62/03632-05XE	<u>4/</u>	TPS76827QPWPREP	76827EP
V62/03632-06XE	<u>4/</u>	TPS76828QPWPREP	76828EP
V62/03632-07XE	<u>4/</u>	TPS76830QPWPREP	76830EP
V62/03632-08XE	01295	TPS76833QPWPREP	76833EP
V62/03632-09XE	01295	TPS76850QPWPREP	76850EP

- 1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.
2/ The PWP package is available taped and reeled. Note R suffix to the device type (e.g., TPS76801QPWPREP).
3/ This device is programmable using an external resistor divider (see manufacturer application information).
4/ This device is not available from an approved source of supply.

CAGE code

01295

Source of supply

Texas Instruments, Inc.
Semiconductor Group
8505 Forest Lane
P.O. Box 660199
Dallas, TX 75243
Point of contact: U.S. Highway 75 South
P.O. Box 84, M/S 853
Sherman, TX 75090-9493

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/03632
		REV	PAGE 12